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APPLICANTS

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** CONTINUING DATA *****

C C
none

** FOREIGN APPLICATIONS *****

C C

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IF REQUIRED, FOREIGN FILING LICENSE GRANTED

** 10/28/2003

Foreign Priority claimed 35 USC 119 (a-d) conditions met	<input checked="" type="checkbox"/> yes <input type="checkbox"/> no <input checked="" type="checkbox"/> yes <input type="checkbox"/> no <input type="checkbox"/> Met after Allowance	STATE OR COUNTRY GERMANY	SHEETS DRAWING 6	TOTAL CLAIMS 21	INDEPENDENT CLAIMS 2
Verified and Acknowledged	<u>C. Chandhok</u> Examiner's Signature	Initials			

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TITLE

Method for fabricating a vertical transistor, and semiconductor memory cell having a trench capacitor and an associated vertical selection transistor

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